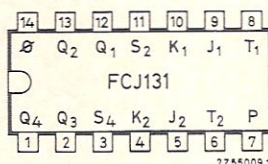
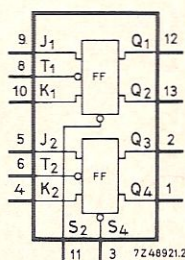


The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

development sample data

DUAL JK MASTER-SLAVE FLIP FLOP



Package XG14; dual in-line

QUICK REFERENCE DATA

Supply voltage	V_P	$6.0 \pm 5\%$	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Clock rate	f_c	typ. 7	MHz
Available d.c. fan out $T_{amb} = 25^\circ\text{C}$	N_a	$\geq$	8
D.C. noise margin $T_{amb} = 25^\circ\text{C}$	M_L	typ. 1.2	V
Power consumption 50% duty cycle, $T_{amb} = 25^\circ\text{C}$	P_{av}	typ. 100	mW

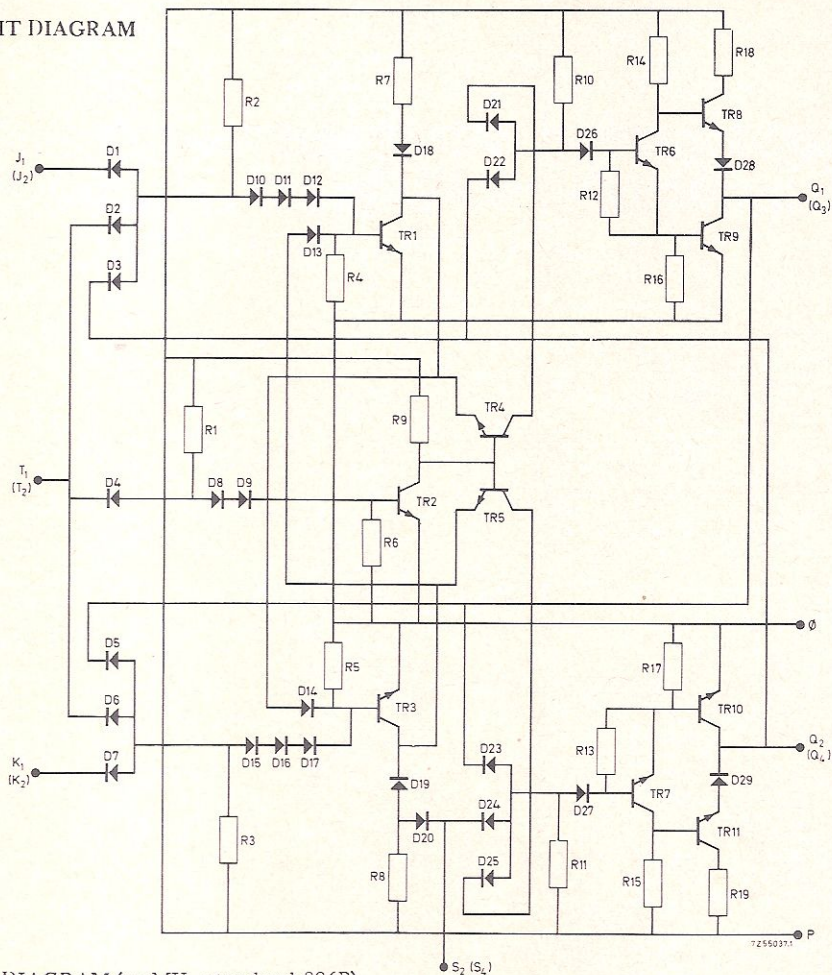
The FCJ131 comprises two independent direct coupled JK flip-flops, operating on the master-slave principle. Operation depends on voltage levels only, i.e. rise and fall times of all input signals, including the trigger signals, are immaterial. The separate set inputs (overriding any other inputs) are active at the LOW level. Typical applications include counters and shift registers.

These data, based on the specifications and measured performance of development samples, afford a preliminary indication of the characteristics to be expected of the described product. Distribution of development samples implies no guarantee as to the subsequent availability of the product

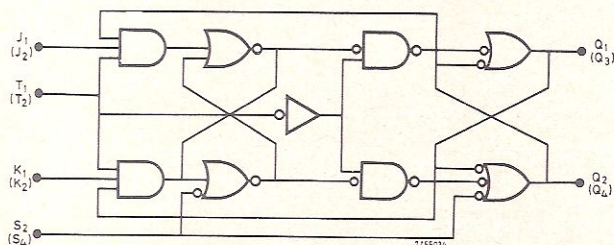
FCJ131
dual flip-flop

FC family
standard temperature range

CIRCUIT DIAGRAM



LOGIC DIAGRAM (to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal (each flip-flop)

T = HIGH		T = LOW	
J ₁	K ₁	Q ₁	Q ₂
J ₂	K ₂	Q ₃	Q ₄
H	H	reversed	
L	H	L	H
H	L	H	L
L	L	no change	

The information on J and K is transferred into the master by T going HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Inputs S₂ and S₄ should be HIGH or floating.

2. Set or reset via S terminals (each flip-flop)

S ₂	Q ₁	Q ₂
S ₄	Q ₃	Q ₄
L	L	H
H	no change	

The set inputs override the other inputs and directly determine the outputs of the relevant flip-flop.

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

RATINGS (Limiting values)¹⁾

Supply voltage	V _P	max.	8.0 V
Output voltage	V _Q	max.	8.0 V
Input voltage	V _J , V _K , V _T , V _S	max.	8.0 V
Output current ²⁾	-I _Q	max.	20 mA
Input current ³⁾	-I _J , -I _K , -I _T , -I _S	max.	20 mA
Voltage difference between any two inputs		max.	8.0 V
Storage temperature	T _{stg}	-55 to +125	°C
Operating ambient temperature	T _{amb}	0 to +75	°C

¹⁾ Limiting values according to the Absolute Maximum System as defined in IEC publication 134.

²⁾ For negative output voltage in LOW state.

³⁾ At this limit input voltages typ. : -1.5 V.

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SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +75 °C
Uniform system supply voltage	V_p	5.7 to 6.3 V
Available d.c. fan out		
to T input	N_{aT}	≥ 3
to J or K input	$N_{aJ} = N_{aK}$	≥ 10
to S input	N_{aS}	≥ 4
to G input	N_{aG}	≥ 8
D.C. noise margin		
to T input	M_L	min. 0.3 V
	M_H	min. 1.3 V
to J or K input	M_L	min. 0.7 V
	M_H	min. 1.3 V
to S input	M_L	min. 0.3 V
	M_H	min. 2.0 V
to G input	M_L	min. 0.4 V
	M_H	min. 1.6 V
Average propagation delay time	t_{pd}	max. 105 ns
Maximum clock rate	f_c	≥ 5 MHz
Equivalent input capacitances		
for T input	C_T	typ. 12 pF
for J or K input	$C_J = C_K$	typ. 4 pF
for S input	C_S	typ. 8 pF
Supply current (duty cycle 50%) ¹⁾	I_{pav}	typ. 16.8 mA
Power dissipation at $T_{amb} = 75$ °C ¹⁾	P_{tot}	max. 150 mW

¹⁾ Both flip-flops together

CHARACTERISTICS

		T _{amb} (°C)			Conditions and references	
		0	+25	+75	V _P (V)	
<u>STATIC DATA</u>						
Output voltage LOW	V _{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3
at:						
Output current LOW	I _{QLmax}	14.0 16.0	16.5 19.0	12.4 14.4	mA	5.7 6.3
Output voltage HIGH	V _{QHmin}	3.9	4.0	4.1	V	5.7
						I _Q = -100 μA
Output voltage HIGH (lowest permissible)	V _{QHPmin}	3.6	3.3	3.0	V	5.7
at:						
Output current HIGH	-I _{QHmax}	0.85	3.3	5.5	mA	5.7
Input current LOW	-I _{JLmax}	1.4	1.3	1.2	mA	5.7
	-I _{KLmax}	1.6	1.5	1.4	mA	6.3
	-I _{TLmax}	4.0	3.8	3.5	mA	5.7
		4.5	4.2	3.9	mA	6.3
	-I _{SLmax}	2.9 3.3	2.8 3.2	2.6 2.9	mA	5.7 6.3
						V _J = V _K = 0.4 V; other inputs floating V _T = 0.4 V; other inputs floating V _S = 0.4 V; other inputs floating
Input current HIGH	I _{JHmax} , I _{KHmax}	1	1	25	μA	5.7
	I _{THmax}	3	3	75	μA	5.7
	I _{SHmax}	2	2	50	μA	5.7
						V _J = V _K = 5.3 V other inputs 0 V V _T = 5.3 V other inputs 0 V V _S = 5.3 V other inputs 0 V
Supply current (both flip-flops together)	I _{Pmax}	-	26.7	-	mA	6.3
						T inputs LOW J, K, S inputs HIGH

CHARACTERISTICS

		T _{amb} (°C)			Conditions and references		
		0	+25	+75	V _P (V)	fig.	
<u>DYNAMIC DATA</u>					5.7 and 6.3		
<u>Change of state</u>							
Input voltage HIGH	V _{THmin} V _{JHmin} V _{KHmin}	2.6	2.3	1.9	V	HIGH level at T and J and/or K to be present simultaneously	1
during: Input time HIGH	t _{THmin}	60	60	60	ns		1
to: T-input voltage LOW	V _{TLmax}	1.0	1.0	0.7	V	t _{TLmin} = t _{pdf}	1
<u>No change of state</u>							
J/K input voltage LOW	V _{JLmax} V _{KLmax}	1.6	1.4	1.1	V	LOW level at J and K to be present prior to T turning HIGH and to remain present during T is HIGH	2
<u>Clock skew protection</u>							
Hold time	t _{hold max}	10	10	10	ns		2
<u>Reset</u>							
S input voltage LOW	V _{SLmax}	1.0	1.0	0.7	V	{ active t _{SLmin} = t _{pdf} inactive	3
S input voltage HIGH	V _{SHmin}	1.9	1.8	1.6	V		
<u>DYNAMIC DATA</u>							
<u>Propagation delay times from T to Q</u>							
Rise propagation delay time	t _{pdr max}	-	90	-	ns	{ V _{pd} = 1.5 V N = 1; C _w = 60 pF	4
Fall propagation delay time	t _{pdf max}	-	120	-	ns		{ V _{pd} = 1.5 V N = 8; C _w = 30 pF other output: N = 1; C _w = 60 pF

CHARACTERISTICS (continued)

DYNAMIC DATA

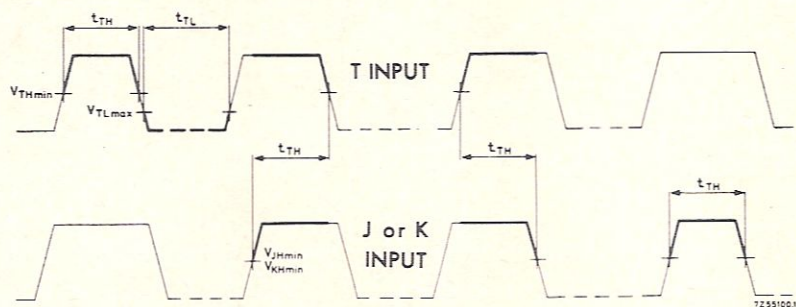


Fig. 1. Waveforms illustrating conditions for change of state.

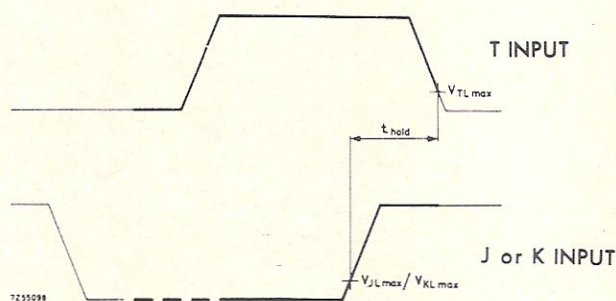


Fig. 2. Waveforms illustrating conditions for no change of state.

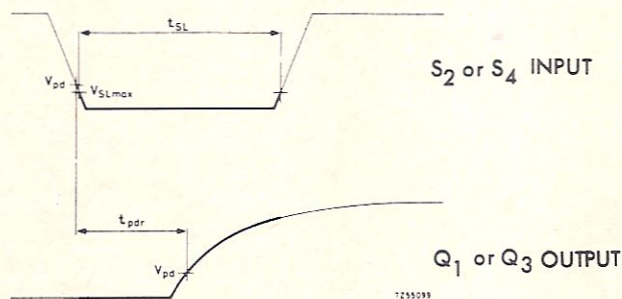
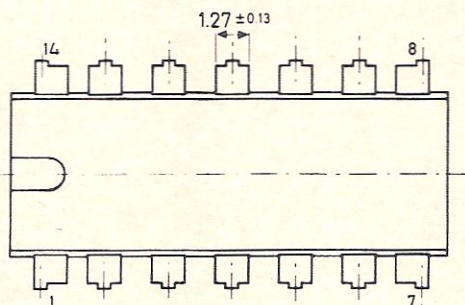
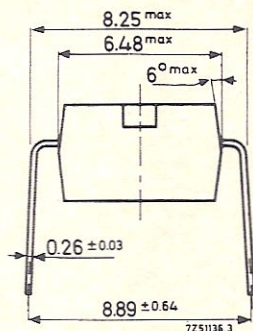
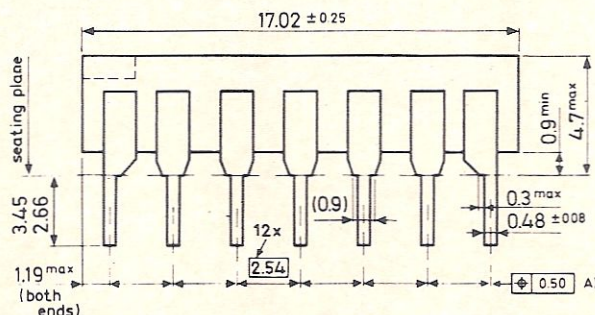


Fig. 3. Waveforms illustrating conditions for set or reset.

PACKAGE OUTLINE
XG14; dual in-line

Dimensions in mm



A) The spacing between center-lines of any two pins is equal to the true position spacing of 2.54 mm per pin with a total tolerance of ± 0.25 mm.

top view

Handling notes

1. Devices may be soldered directly into circuits with soldering irons. At iron temperatures below 245°C the maximum soldering time should be less than 10 seconds and at iron temperatures between 245°C and 400°C the soldering time should be less than 5 seconds. In both cases the soldering iron should be applied below the seating plane (see outline drawing).
2. Devices mounted up to the seating plane on a printed circuit board may be dip or flow soldered providing the solder temperature is below 245°C and the time of immersion is less than 5 seconds. The body temperature should not be allowed to exceed the maximum storage temperature during soldering. If excessive pre-heat cycles are used, it may be necessary to cool the printed board immediately after leaving the solder bath/wave in order that this requirement is met.

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